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A PROPOSED DESIGN TO REDUCE HIGH POWER CONSUMPTION IN FBMC TRANSMISSION SYSTEMS

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Abstract

A higher data rate with lower intersymbol interference (ISI) and intercarrier interference (ICI) are the main features provided by Filter bank multi-carrier (FBMC) modulation technique to be the most candidate for 5G wireless networks. Although the different advantages of FBMC systems, it suffers from the higher power consumption and complexity of the structure, as a result of using fast Fourier transform/ inverse fast Fourier transform (FFT/IFFT) processors with a high order polyphase filter network in both transmitter and receiver. This paper presents a complete analysis, design, and implementation of a proposed low power FBMC transceiver architecture for a different number of multi-users or subscribers. The suggested method aims to reduce power consumption and area resources by reducing the complexity of the FFT (2^n Points) processor by using a feedback loop with a (n) points FFT core. Also, the design of FIR filters is based on distributed arithmetic (DA) algorithm in which all multiplications and additions are replaced by a table and a shifter. The design and implementation are done using a Xilinx system generator tool and spartan-6 field programmable gate array (FPGA) board. The proposed implementation method presents a reduction in resources by 15 % compared to conventional implementation.

Keywords: FBMC, FFT, FPGA, Power Consumption

Introduction

The future mobile technology (5G) is expected to meet the requirements of higher data rate, and an extra number of users, which requires the more efficient use of the frequency spectrum, to fulfil with these new requirements several modulation schemes proposed by researchers. Orthogonal division multiple access (OFDM), is the most modulation technique in broadband wired and wireless systems [1]. OFDM Also used in the broad class of DSL standards and the majority of wireless standards such as variations of IEEE 802.11 and IEEE 802.16, 3GPP-LTE, and LTE-Advanced [2]. Unfortunately, OFDM has many drawbacks make it not suitable for the 5G specification, so it is essential to search for another modulation technique for 5G technology.

As the name implies, FBMC uses for digital multicarrier modulation. The main benefits in the utilization of this type of

modulation are the minimization of inter symbolic interference (ISI) and intercarrier interference (ICI) that may introduce when using channels with a varying gain in their frequency band. This minimization is possible because the use of multicarrier modulation eases the task of channel equalization, which is used to diminish the effects of the ISI and ICI [3].

Another most critical advantages of FBMC is its higher spectral efficiency when compared with OFDM systems [4]. FBMC don't use a cyclic prefix (CP), so it increases this performance, as CP originates additional overhead and, as a consequence, a loss in bandwidth efficiency. Also, OFDM systems present strong side lobes in their frequency response, while FBMC has a lower side lope. Side lobes in FBMC are considerably smaller than the ones obtained with OFDM [5].

The higher selectivity and spectral containment of FBMC subchannels also contribute to achieving good resistance when faced with narrowband interference. It has been calculated that FBMC presents a 20% gain in spectral efficiency when compared to OFDM. FBMC's transceiver consists of, an offset quadrature amplitude modulation (OQAM) modulation block, followed by a synthesis filter bank (SFB) in the transmitter, while in the receiver it has analysis filter bank (AFB), and an OQAM demodulation block, as shown in Fig.1 [6].

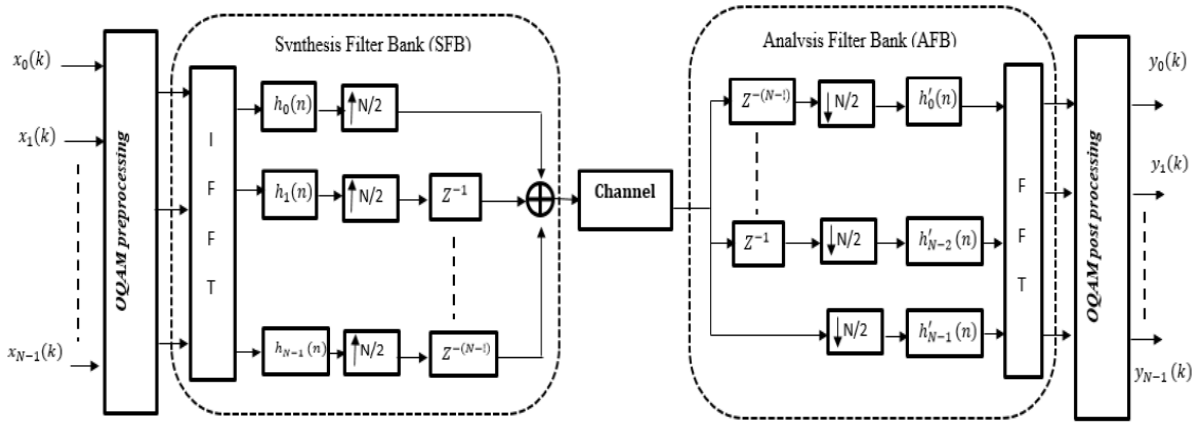

Fig.1 FBMC Generic system.

Implementation of SFB is done by using IFFT followed by polyphase network (PPN) and AFB is implemented by PPN followed by FFT. PPN block consists of a set of filters which, when combined, form the impulse response of a prototype filter which can be configured in such a way to achieve better localization in the frequency domain. The shape and length of the prototype filter will change the time and frequency domain localization [7]. From Fig. 1, PPN in the SFB in the transmitter consists of N number of finite impulse response (FIR) filters. Each FIR filter output is followed by (N/2) upsamplers and delay units. All filters output are summed to form the transmitter signal. While PPN in AFB in the receiver consists of delay units, downsamplers (N/2), N FIR filters, and FFT processor. The filter banks have the following characteristics:

1) The number of subchannels is even number, although it is common to use a power of 2, as it is one of the conditions for some efficient IFFT algorithms;
2) The filter length should be given by : L = KM

where L is the filter length, K the overlap factor and M the number of subcarriers used.

Having defined the values of L, M, and K to design the prototype filter one can use the frequency sampling technique to obtain the filter coefficients.

It is seen in Fig. 1, implementation of FFT, IFFT, and FIR filters require a large number of multipliers and adders which causes a high power consumption and reduce the speed of operation. It is clear from the structure of FBMC architecture that, the implementation method of FFT, IFFT, and FIR filters determines the power consumption and speed of the entire architecture. The FFT algorithm should be chosen here to consider the execution speed, hardware complexity, and flexibility and precision, while the FIR implementation algorithm should be chosen to reduce the complexity of the design, reduce power consumption.

In this paper, we present a complete design and implementation of low power FBMC transceiver architecture. The proposed architecture presents a new method to implement FFT/IFFT processors which reduces the complexity and number of multipliers and adders compared to traditional FFT/IFFT processors. The proposed architecture also implemented FIR filters with a method in which no multipliers are used and replace them with adders and shifters, which reduces the power consumption. The proposed modifications reduce the overall power consumption, enhance the speed, and reduce the hardware utilization for implementation.

Proposed FBMC Transceiver

A. Modulation Technique with FBMC

Quadrature Amplitude Modulation (QAM) as a modulation technique with FBMC leads to a lower spectral efficiency as orthogonally between subcarriers is obtained through a reduction in the frequency domain overlap. While OQAM technique, obtain orthogonally in the real domain only, which guarantees maximum spectral efficiency. The use of OQAM modulation also has the impact of doubling the processing rate of the system. As a consequence of its better spectral performance OQAM based FBMC implementations are considered as the baseline modulation for FBMC [8].

B. FFT Processor

The main constraints for designing FFT/IFFT cores are power consumption and time. For example in WI-FI (IEEE 802.11x), the time constraints to finish FFT/IFFT calculations is 89.6 μs. The cost to fulfill time constraint is the complexity of the architecture which, increase the area and power consumption. FFT is used to perform the discrete Fourier transform (DFT), it reduces the computation time, and reduce the number of multipliers and adders used to implement the transform.

Different algorithms, such as radix-4, split radix to avoid radix-2 structure aim to reduce the complexity of FFT the algorithm. These architectures are either based on the Decimation-in- Time (DIT) or on the Decimation-in-Frequency (DIF). Several designs based on these architectures were proposed in order to

implement these algorithms and to reduce complexity of DFT structure [9 - 10].

The proposed DFT processor is designed for (N) points that is power of 4 such as (4, 16, 64, 256, ……). In the following mathematical model we will use $N = 256$. The conventional 256- points FFT/IFFT processor can be described using DFT with the following Eqn:

$$X[k] = \sum_{n=0}^{255} x(n).W_{255}^{nk} \quad (1)$$

Where: W is the twiddle factor, $W_N^{nk} = e^{-\frac{j2\pi nk}{N}}, 0 \le k \le N-1$

The new method can be described with the following equation:

$$X[r + t\ d] = \sum_{k=0}^{t-1}[W_N^{rk}\ \sum_{m=0}^{t-1} x[k + tm].W_t^{rm}]W_t^{kd} \quad (2)$$

With : N=256; t=16

Where: $r, k \in \{0,1, \dots ,15\}$ and $m, d \in \{0,1, \dots ,15\}$

The idea of proposed method is to use a 16-point FFT processor as a core of feedback system to form a 256-point processor. The description steps of calculation can be explained simply as :

1- Receive the input 256- point.
2- Separate the input 256- points into 16 groups of 16-points each, in the right order to calculate the 1st FFT using 16-point FFT core processor.
3- The output points of the 16-point processor are multiplied by the predefined twiddle factors.

Collect the complete 256- points in a register fed them again as input and prepare them to calculate the 2nd FFT using 16-point FFT core processor. The final result (256 points) is collected into the register without multiplying by predefined twiddle factors.

The main idea of 256- point FFT/IFFT architecture is shown in Fig. 2, it consists of an order block, 16-point FFT processor, multiplier, and register. The order block receives the input 256 points, arrange them in the suitable order for FFT processor, send out 16 points in each clock pulse to FFT block. Also, order block generates two control signals, the first is wait signal, this signal as default equal to ‘1’ and this means we still in the 1st FFT loop, so the 16 points generated from 16 points FFT processor multiplied by twiddle factors using a multiplier. When it equal to ‘0’ the output goes directly to the output register without multiplying to twiddle factors.

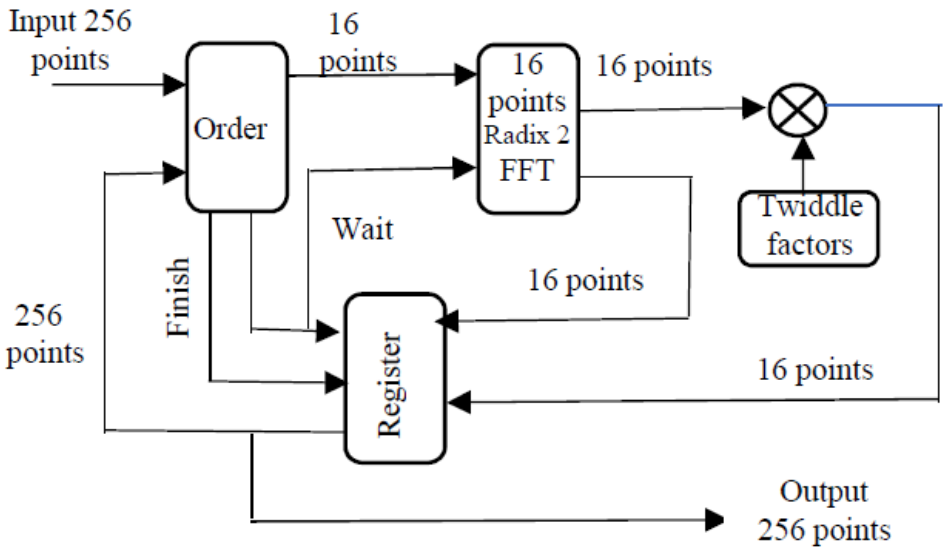

Fig. 2 The proposed modified FFT processor.

The second control signal is finished signal. It by default equal to '0' and means the output of the register block directed to order block, when it equal to '1' it means the final result is ready to go to the output of the core. Both wait and finish signals are controlled by a counter. The 16-point FFT processor, which is the core of the 256-points FFT has four stages pipelined structure carrying out 24 real multiplications, and eventually processes 16-points FFT. The multiplier block, multiply the input 16 point by the predefined twiddles factor. The multiplications are done only for the first loop.

The complex multiplication is the most expensive arithmetic operation and power consumption in FFT architecture. In the proposed architecture, to reduce the multiplication complexity between the input point and the twiddle factors, the complex multiplication is replaced by three real multipliers and three adders/subtractor. The complex twiddle factor multiplication can be described for the input (A+ jB) as follows:

$$r + jI = (A + jB).W_N = (A + jB)(C + j\,D) \quad (3)$$

It can be simplified:

$$r = (C - D)B + C(A - B) \quad (4)$$

$$I = (C + D)A - C(A - B) \quad (5)$$

Using this method we store the values C, C-D, C+D in a (LUT) and prepare these values to be used in Eqns (4,5). As indicated in Eqns(4,5) the result of multiplying the input by the twiddle factor is done using three real multipliers and three adders/ subtractors. The number of twiddle factors saved in LUT is the half of them (128 points), and the others are the negative of the stored factors since $W_{256}^{0:127} = -W_{256}^{128:255}$. The proposed processor requires less number of arithmetic operations compared to the conventional Cooley-Tukey algorithm, and to efficient processors implemented in pipeline structure with radix-2, radix-2, radix-4 and split-radix algorithm for a different number of points. This comparison is shown in Table 1. Hence the

proposed method achieve fewer hardware resources compared to different algorithms.

C. Filter Bank

FIR filters are the most elementary elements in FBMC architecture. The basic building blocks of FIR filter are multiplier, adders and signal delay. Multipliers should be fast enough so that overall throughput should not suffer. Adders are used in combination of multipliers and delays are used to store sample value in memory for one sample clock cycle. FIR has two most commonly used structures, direct form and transposed form. In the direct form, several signals multiplied by constants and added afterwards. But for accomplishing high throughput and reduction in delay of the adder, it requires extra pipeline register between adders. On the contrary, transposed form have a register between adders. Also, it gains high throughput without additional pipeline registers. FIR filter architecture consumes much power since it has a large number of multipliers, adders, and subtractors.

Distributed Arithmetic (DA) is a different approach to implement digital filters. The basic idea is to replace all multiplications and additions by a table and a shifter-accumulator. DA relies on the fact that the filter coefficients $c[n]$ are known, so multiplying $x[n]c[n]$ becomes a multiplication with a constant. This is an importance difference and a prerequisite for a DA design [11-12]. DA uses Lookup Table (LUT) to store the pre-computed result to reduce computational complexity. It uses Read Only Memory (ROM) based LUT to store the result in case of fixed coefficients. This method explains efficient design for implementation of shared LUT realization of FIR filter using distributed arithmetic approach. A block diagram for the DA implementation of a FIR filter is shown in Fig. 3.

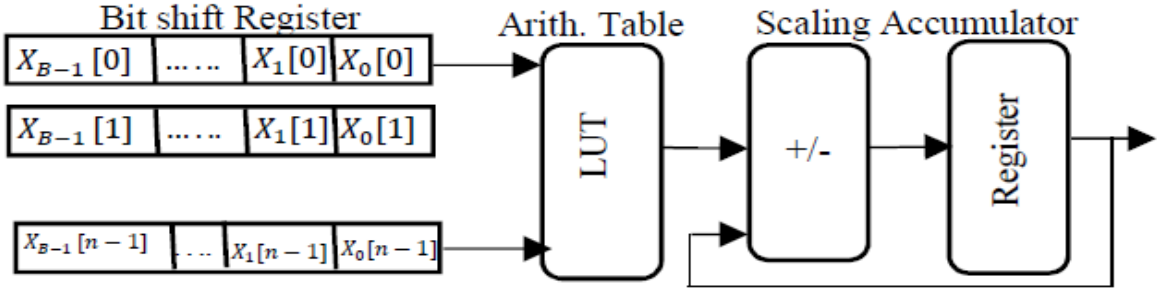

Fig. 3 DA implementation block diagram.

Table 1. Comparison Between Real Multiplications and Adders in Different Algorithms and Lengths

Architecture	**Real Multiplication**		**Real Add/Sub**	
	N=16	***N=256***	***N=16***	***N=256***
Cooly-Tukey	128	6144	192	10240

Architecture	Real Multiplication		Real Add/Sub	
	N=16	***N=256***	***N=16***	***N=256***
Radix-2MDC	28	1800	148	5896
Radix-4MDC	20	1392	148	5488
Split-Radix MDC	20	1284	148	5380
Radix-2 SDF	24	1800	152	5896
Radix-4 SDF	24	1392	148	8596
Radix-2^2 SDF	24	1392	152	5896
Split-Radix-SDF	20	1284	148	5380
Our Method	16	660	154	5904

FPGA of Low Power FBMC

The FMBC architecture is designed and realized using Xilinx system generator tool which generates VHDL code, while the architecture is implemented using Xilinx Spartan-6 XC6SLX45 FPGA board. The specifications of FBMC architecture are listed in Table. 2.

Table 2. Proposed FBMC Architecture Specification

Parameter	**Value**
Total Bandwidth (B)	5 MHz
Sub-channel separation	700 kHz, 175 kHz, 43.75 kHz
Sample rate	1.6 MHz
Number of subscribers= Sub channels (M)	16, 64, 256
Overlapping factor (K)= M K	4
Filter length (L= M K)	64, 256, 1024

Fig. 4 shows the top level model of FBMC transmitter realized in the Xilinx system generator. The top-level architecture consists of the following blocks: OQAM modulation, IFFT, and FIR. The input data is modulated using an OQAM modulator, and then it passes to the proposed IFFT processor. IFFT is implemented with different lengths 16 points which use 4 point FFT core processor, 64 points which use 8 point FFT core processor, and 256 points which uses 16 point FFT core processor. The AXI FIFO block is used to buffer the frame based output of the FFT to the sample based input of the FIR. Fig. 5 shows the top level of FBMC receiver.

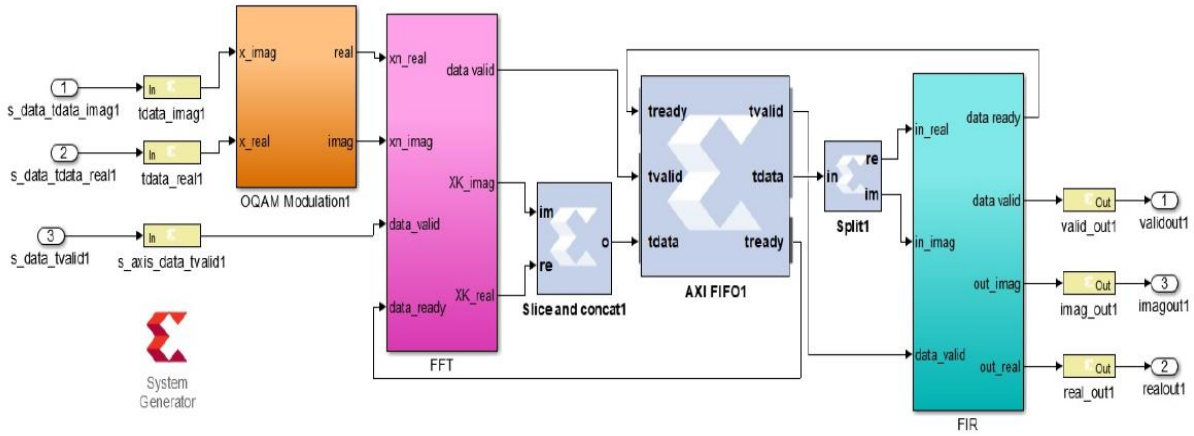

Fig. 4 Top level of proposed FBMC transmitter.

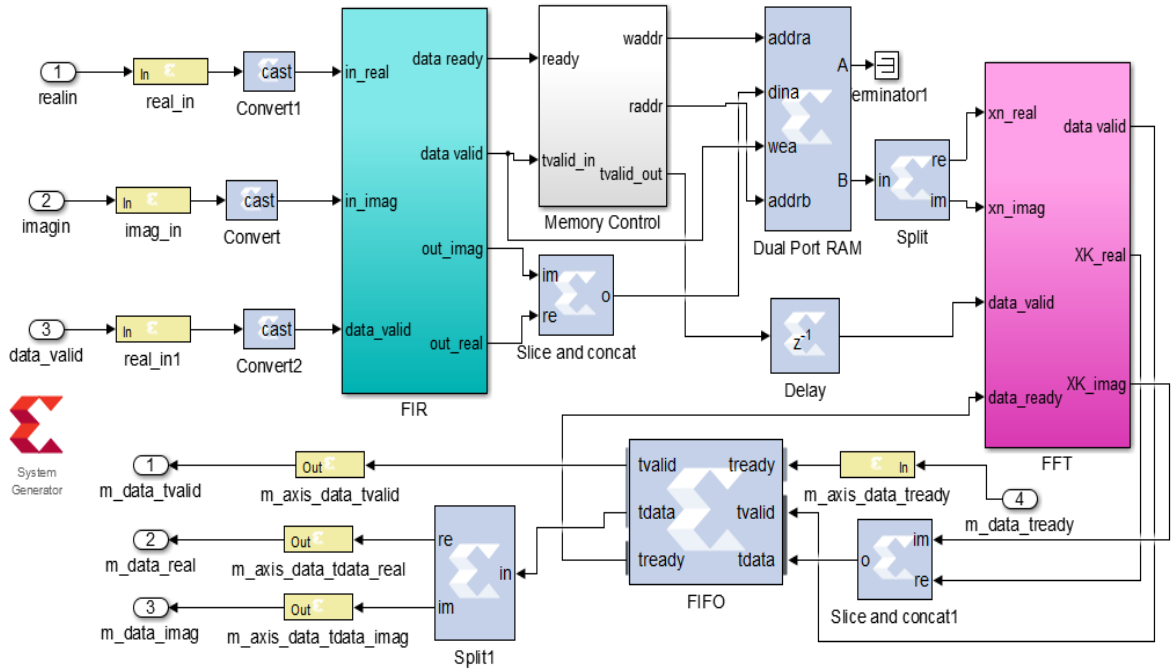

Fig. 5 Top level of proposed FBMC Receiver.

The input data source is complex sinusoidal samples for different 16 sub-channels. The input samples are generated at the symbol rate, which is exactly 1.6 MHz. The proposed IFFT processor is shown in Fig. 6. The proposed FFT processor implemented with different lengths M=16, 64, 256 The implementation results of the proposed FFT processor compared to the conventional radix-2 method is shown in Table 3.

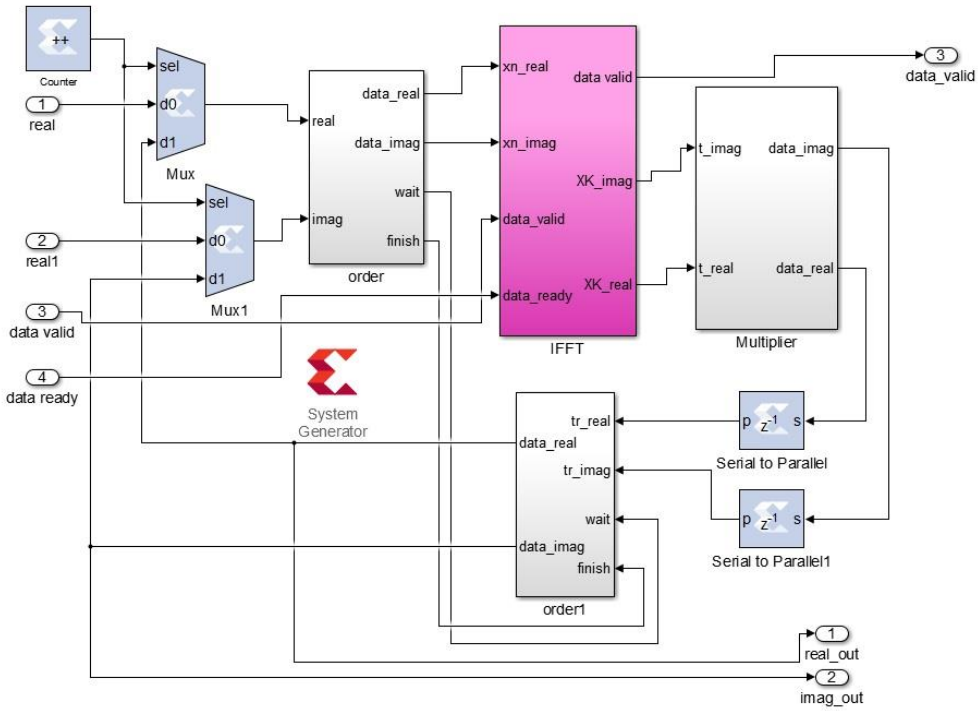

Fig 6 Proposed hardware model for FFT processor.

Table 3 Implementation Results Comparison for Different FFT Lengths

No. of Users		**No. of Slice Register**	**No. of Slice LUTs**	**No. Of fully used LUT-FFs**	**Max. Clock (MHz)**
M=16	Conventional	158	331	479	300
	Proposed	100	115	205	298
M=64	Conventional	320	598	905	290
	Proposed	205	322	780	287
M=128	Conventional	1008	2120	3230	260
	Proposed	856	1580	2640	258

The prototype filter is designed to operate at the sample rate of the higher frequency stream but has a passband less than or equal to the Nyquist frequency of the input/output sub-channels. The filter is used to suppress the aliasing introduced by the up/down sampling process. The filter coefficients are generated using Matlab, with a passband frequency of 90 kHz and stopband frequency 100 kHz. The implementation of FIR filter using the DA method (M=8, L=32) is shown in Fig. 7, while the used resources compared to the conventional method shown in table 4. The output spectrum of FBMC transmitter is shown in Fig.8; it is seen that it has 16 sub-channel with 100 kHz bandwidth each.

Table 4 Implementation Results for Different DA FIR Lengths

Filter length		No. of Slice Register	No. of Slice LUTs	No. Of fully used LUT-FFs	Max. Clock (MHz)
L=64	Conventional	220	419	510	245
	Proposed	150	305	420	298
L=256	Conventional	480	990	1020	227
	Proposed	310	803	890	287
L=1024	Conventional	989	1520	2487	208
	Proposed	846	2487	1997	258

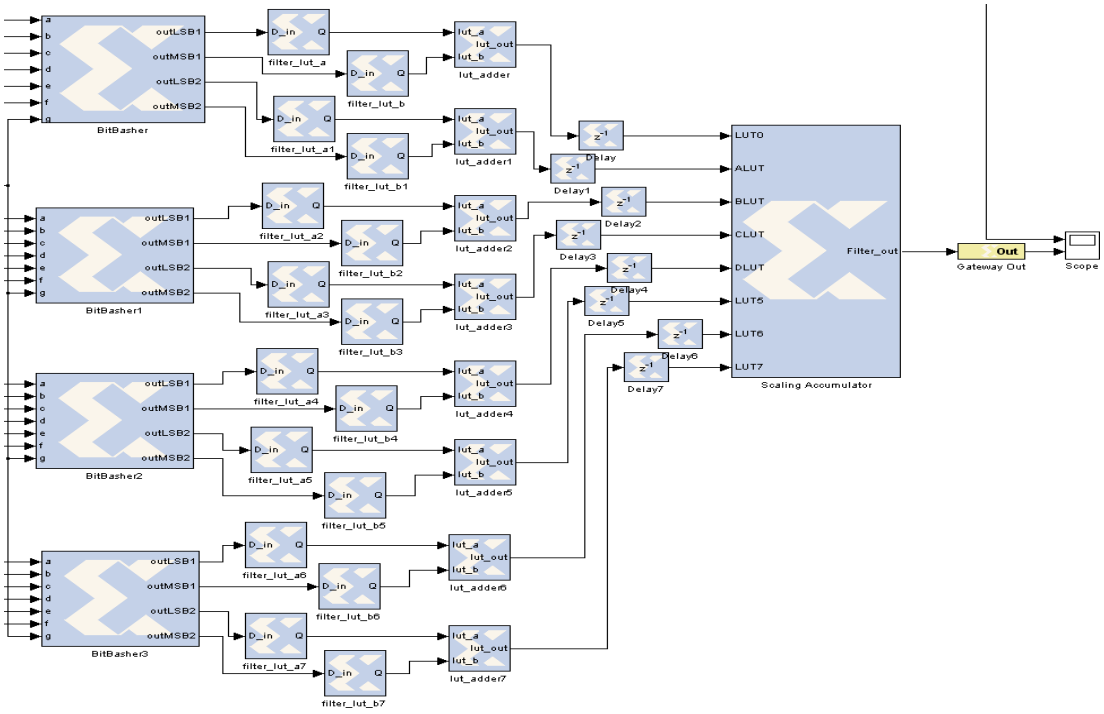

Fig. 7 Hardware model of DA FIR.

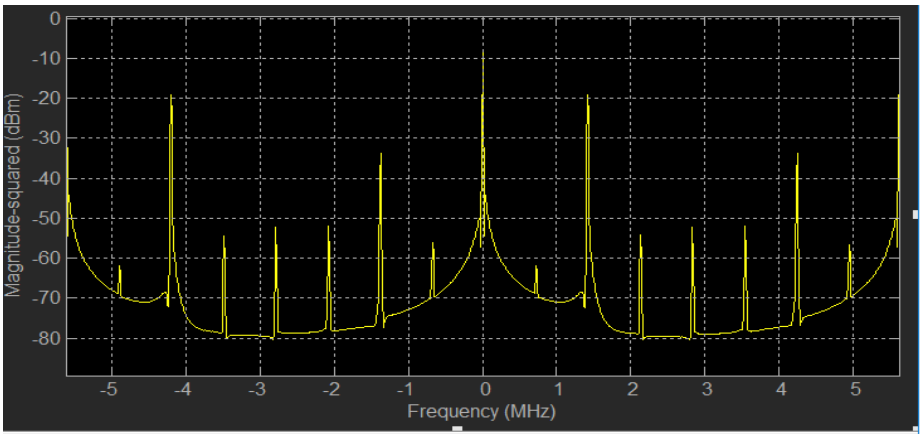

Fig. 8 Transmitter output spectrum.

The resources used for the transmitter and the receiver are shown in table 5 and table 6 respectively. It is noted that the receiver path is more complicated because the first input sample to the receiver must be applied to the last sub-filter and the last FFT bin. The FFT expects its first input sample to be for the first bin. Therefore, the data must be buffered into blocks of 16 samples, and the order of the samples flipped. This reordering is done following the FIR instance. The FIR is configured to apply the sub-filters in reverse order. The reordering is implemented using a Distributed Memory Generator instance along with a counter and some control logic. Finally, the receiver uses a FIFO on the output of the FFT instance to convert between its frame-based output to the desired sample-based channel output.

Table 5. Implementation Results for FBMC Transmitter

No. of Users		**No. of Slice Register**	**No. of Slice LUTs**	**No. Of fully used LUT-FFs**	**Max. Clock (MHz)**
M=16	Conventional	398	755	995	238
	Proposed	270	425	631	235
M=64	Conventional	820	1593	1931	219
	Proposed	535	1128	1676	215
M=256	Conventional	2017	3645	5723	208
	Proposed	1722	2815	4643	205

Table 6. Implementation Results for FBMC Receiver

No. of Users		**No. of Slice Register**	**No. of Slice LUTs**	**No. Of fully used LUT-FFs**	**Max. Clock (MHz)**
M=16	Conventional	448	810	1078	238

	Proposed	298	481	703	235
M=64	Conventional	905	1640	2070	219
	Proposed	620	1250	1750	215
M=128	Conventional	2105	3735	5810	208
	Proposed	1802	2905	4726	205

Conclusion

In this paper, a modified design and implementation of low power consumption FBMC system has been presented by replacing the conventional FFT processor, and FIR filter design. The proposed FFT reduces the total number of multipliers and adders used in a conventional FFT processor. The design of FIR filters used in both SFB and AFB is implemented using the distributed arithmetic algorithm in which no the multipliers and adders are replaced by a table, and a shifter is used. A complete design of modified FBMC system using a lot of modifications is implemented using Xilinx Spartan-6 FPGA. Different implementations of the FBMC system with a different number of subscribers (M), and different filter lengths (L) are done to investigate the reduction in consumed resources which leads to reduce power consumption due to the modifications.

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